Claims

The claims are amended as follows:

1. (Currently Amended) A matrix switch comprising:

an input port for splitting a plurality of virtual output queues (VOQs) into a plurality of VOQ groups, and inputting them;

a plurality of crossbar switch units for independently arbitrating the input VOQ groups, and outputting cells, wherein each crossbar switch unit includes a buffer storing a predetermined sized cell and includes a grant arbiter that outputs a log(n) sized signal based on a selected request signal, the log(n) sized signal representing location information of a selected input port for generating a grant signal;

a plurality of buffers for storing a predetermined sized cell; and

a plurality of output ports for independently arbitrating the cells output from the crossbar switch units, and transmitting the cells to the output ports,

wherein each output port uses credit information that is status information of the corresponding buffer to independently arbitrate the cells,

wherein a first output port which has a first credit value with full state of buffer does not transmit ~~a~~ the grant signal to a first input port which sends a request signal to the first output port, and

a second output port which has a second credit value with no full state of buffer selects one among second input ports, which ~~send~~sent a request signal to the second output port, and the second output port transmits the grant signal to one selected second input port.

2. (Original) The matrix switch of claim 1, wherein part of the crossbar switch units form a plurality of switch modules, and

the switch module further comprises a buffer for storing a predetermined cell in the output port of the crossbar switch unit.

3. (Original) The matrix switch of claim 1, wherein n VOQs are separated into L VOQ groups when N VOQs are provided,

the switch module comprises L crossbar switch units,

the matrix switch comprises L switch modules, and L=N/n where N, L, and n are natural

numbers.

4. (Original) The matrix switch of claim 3, wherein the crossbar switch unit comprises n distributed grant arbiters, n distributed accept arbiters, and a crossbar switch controller,

the grant arbiter receives an n-bit request signal vector from the VOQ, and transmits an n-bit grant signal vector to the accept arbiter, and

the accept arbiter receives the n-bit grant signal vector, and transmits an n-bit accept signal vector to the crossbar switch controller.

5. (Original) The matrix switch of claim 4, wherein the matrix switch further comprises a buffer controller and an output arbiter,

the buffer controller checks the buffer's state, and transmits request signals to the output arbiter when a cell is provided in the buffer, and

the output arbiter selects one of the transmitted request signals, and transmits an accept to the crossbar switch unit.

6. (Currently Amended) An arbitration method of a matrix switch including a plurality of input ports, a plurality of crossbar switch units, a buffer, and a plurality of output ports, comprising:

(a) a grant arbiter of the crossbar switch unit searching for request signals transmitted from the input ports, and selecting the first-requested input port, the grant arbiter outputting a log(n) sized signal based on a selected request signal, the log(n) sized signal representing location information of the selected first-requested input port for generating a grant signal;

(b) determining whether a buffer of the output port corresponding to the grant arbiter can receive an additional cell, wherein the determination is based on credit information that is status information of the buffer of the output port;

(c) transmitting ~~a~~ the grant signal to the input port when the buffer can receive the cell;

(d) an accept arbiter of the crossbar switch unit selecting the first-granted grant signal of the grant signals; and

(e) the accept arbiter transmitting an accept signal to the output port corresponding to the selected grant signal,

wherein in step (c), a first output port which has a first credit value with full state of buffer does not transmit a grant signal to a first input port which sends a request signal to the first output port, and a second output port which has a second credit value with no full state of buffer selects one among second input ports which send a request signal to the second output port and transmits the grant signal to one selected second input port.

7. (Original) The arbitration method of claim 6, further comprising:

(f) an output arbiter of the output port searching for the request signals transmitted from the crossbar switch unit to select the first-requested crossbar switch unit; and

(g) the output arbiter transmitting an accept signal to the selected crossbar switch unit.

8. (Original) The arbitration method of claim 6, wherein the searching is performed from the predefined highest priority value using the round robin in (a), (d), and (f).

9. (Previously Presented) The arbitration method of claim 8, wherein (c) further comprises updating the new highest priority value based on port information of the selected output port, and storing the value in a register, when the accept arbiter has received a grant signal; and

(h) further comprises updating the highest priority value based on information on the corresponding crossbar switch unit, and storing the value in the register, when the output arbiter has transmitted the accept signal to the crossbar switch unit.

10. (Original) The arbitration method of claim 9, wherein the accept arbiter updates the preset highest priority ranking value by adding 1 to output port information matched with a grant signal, and

the accept arbiter updates the highest priority ranking value preset to the grant arbiter and the output arbiter by adding 1 to input port information and crossbar switch unit information corresponding to the accept signal.